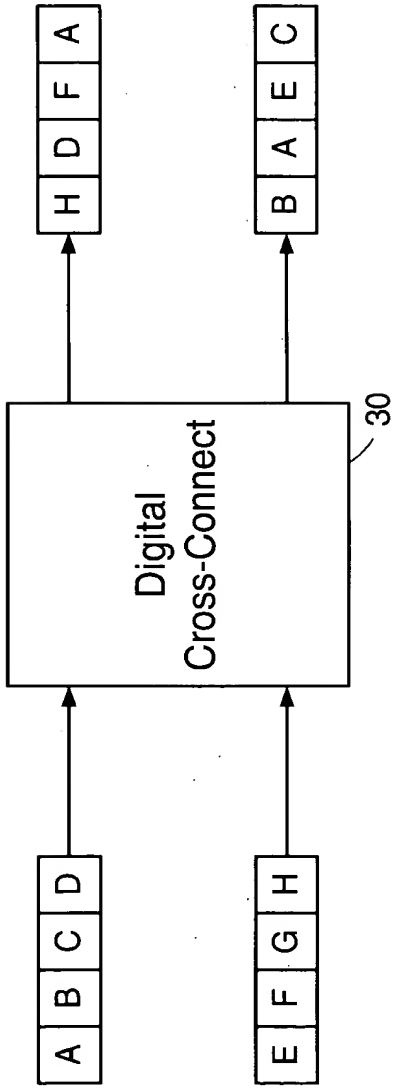

FIG. 1
PRIOR ART

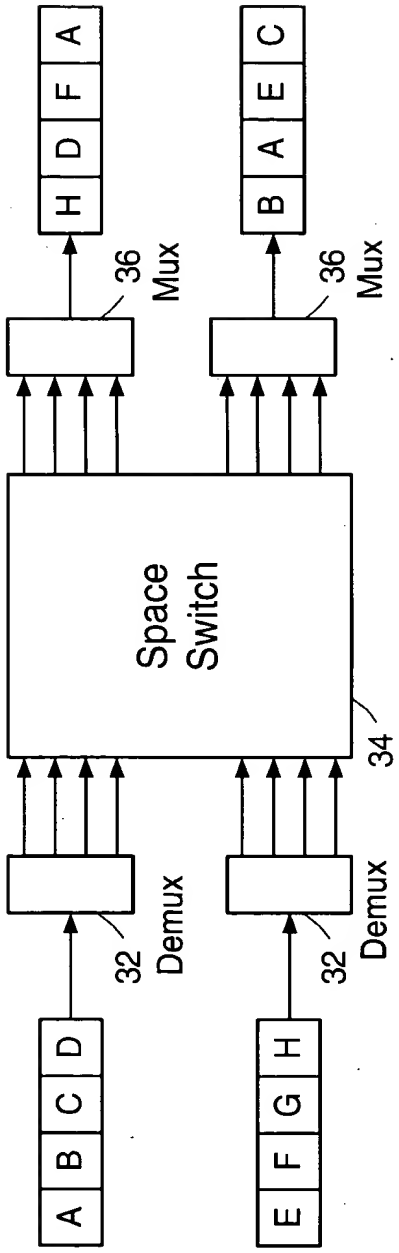

FIG. 2
PRIOR ART

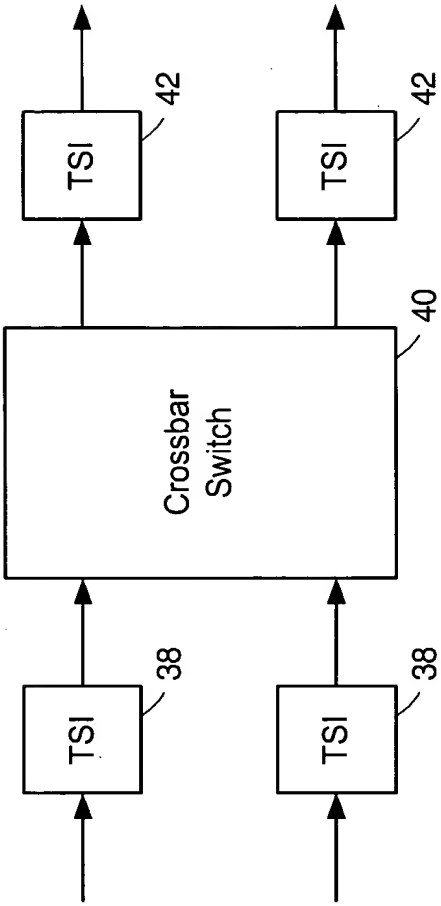

FIG. 3
PRIOR ART

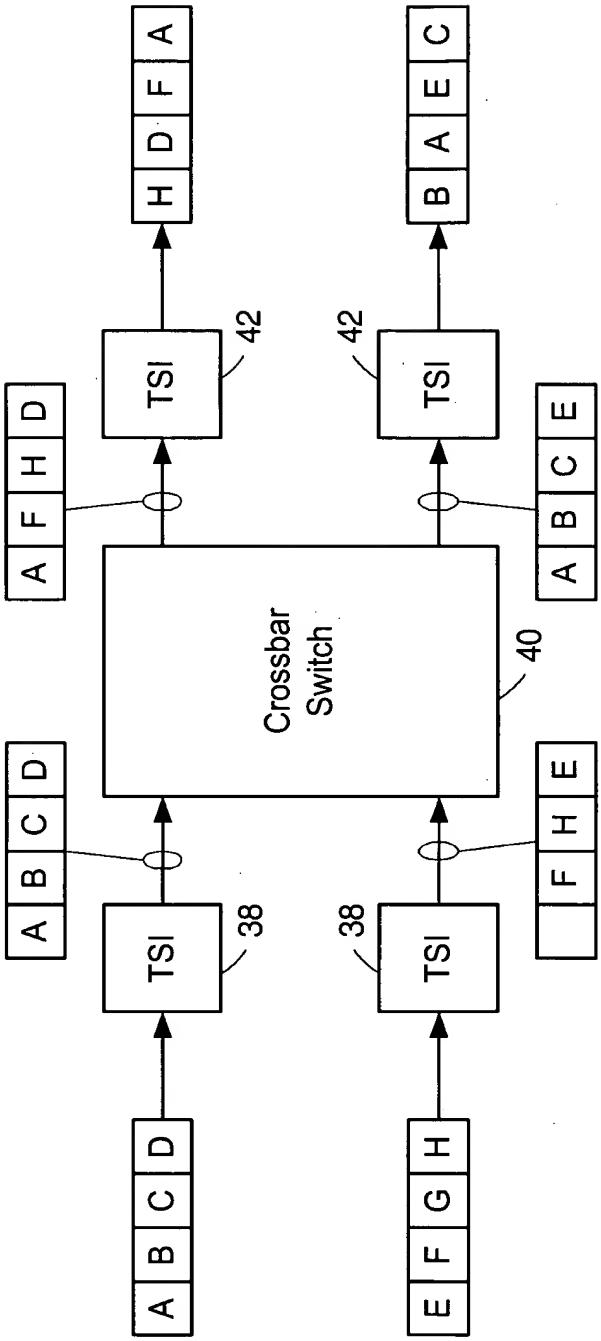

FIG. 4
PRIOR ART

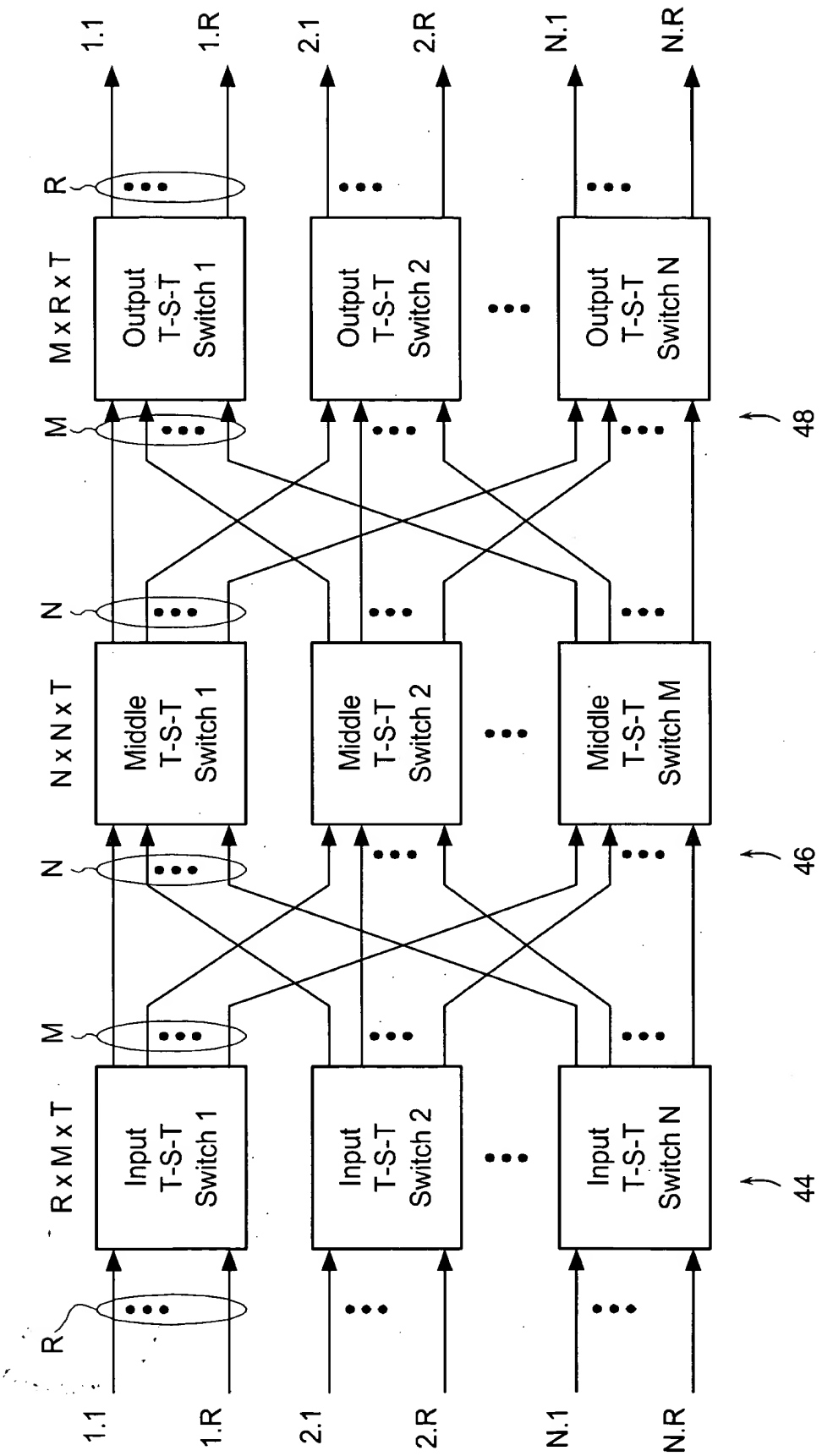
1.1
1.R
2.1
2.R
N.1
N.R
R
M x R x T
Output T-S-T Switch 1
Output T-S-T Switch 2
Output T-S-T Switch N
M
48
N
N x N x T
Middle T-S-T Switch 1
Middle T-S-T Switch 2
Middle T-S-T Switch M
N
46
M
R x M x T
Input T-S-T Switch 1
Input T-S-T Switch 2
Input T-S-T Switch N
R
44
1.1
1.R
2.1
2.R
N.1
N.R

FIG. 5

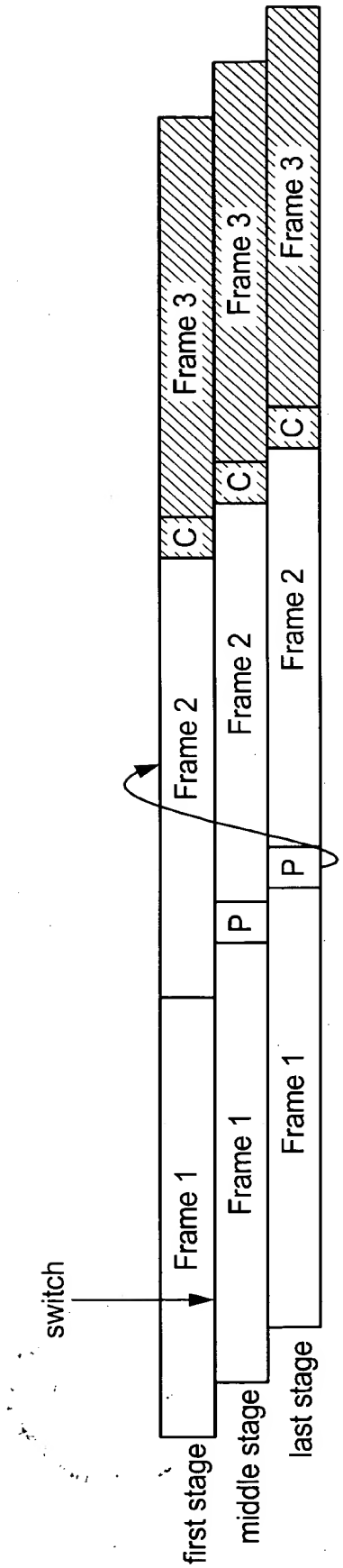

FIG. 6

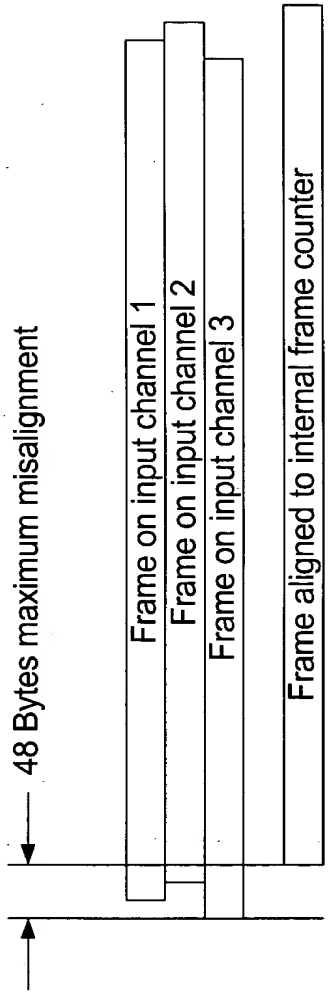

FIG. 13

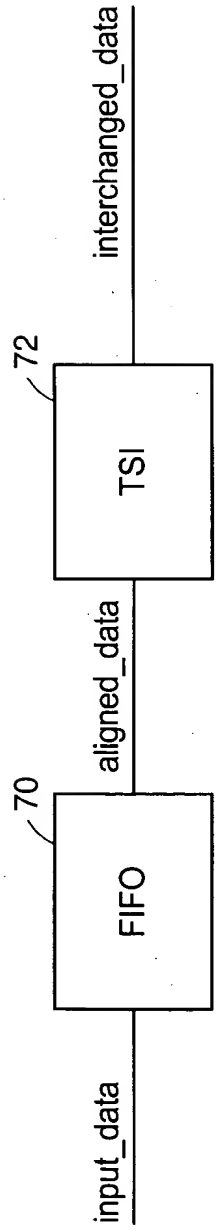

FIG. 14
PRIOR ART

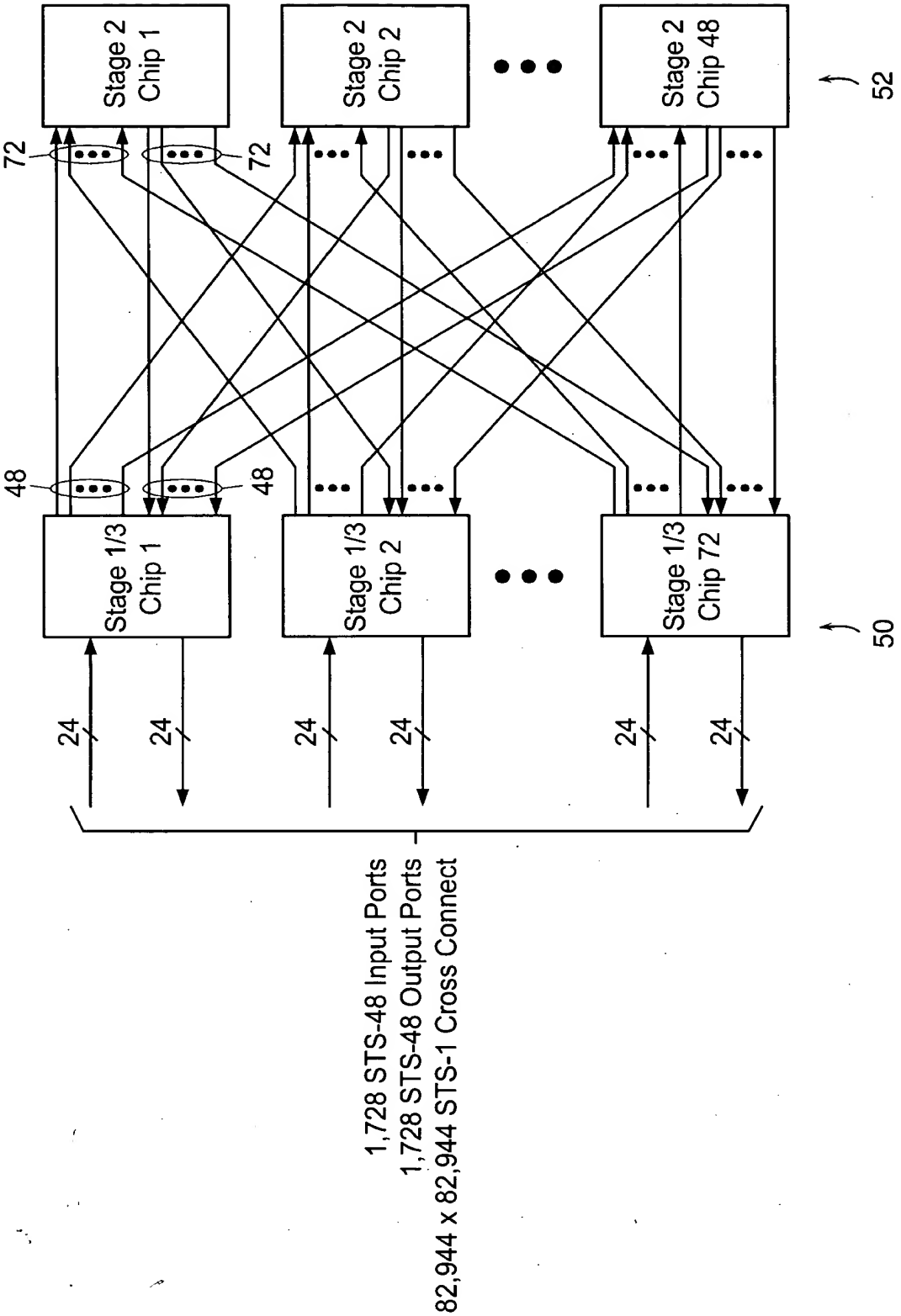

FIG. 7

Page 5 of 16

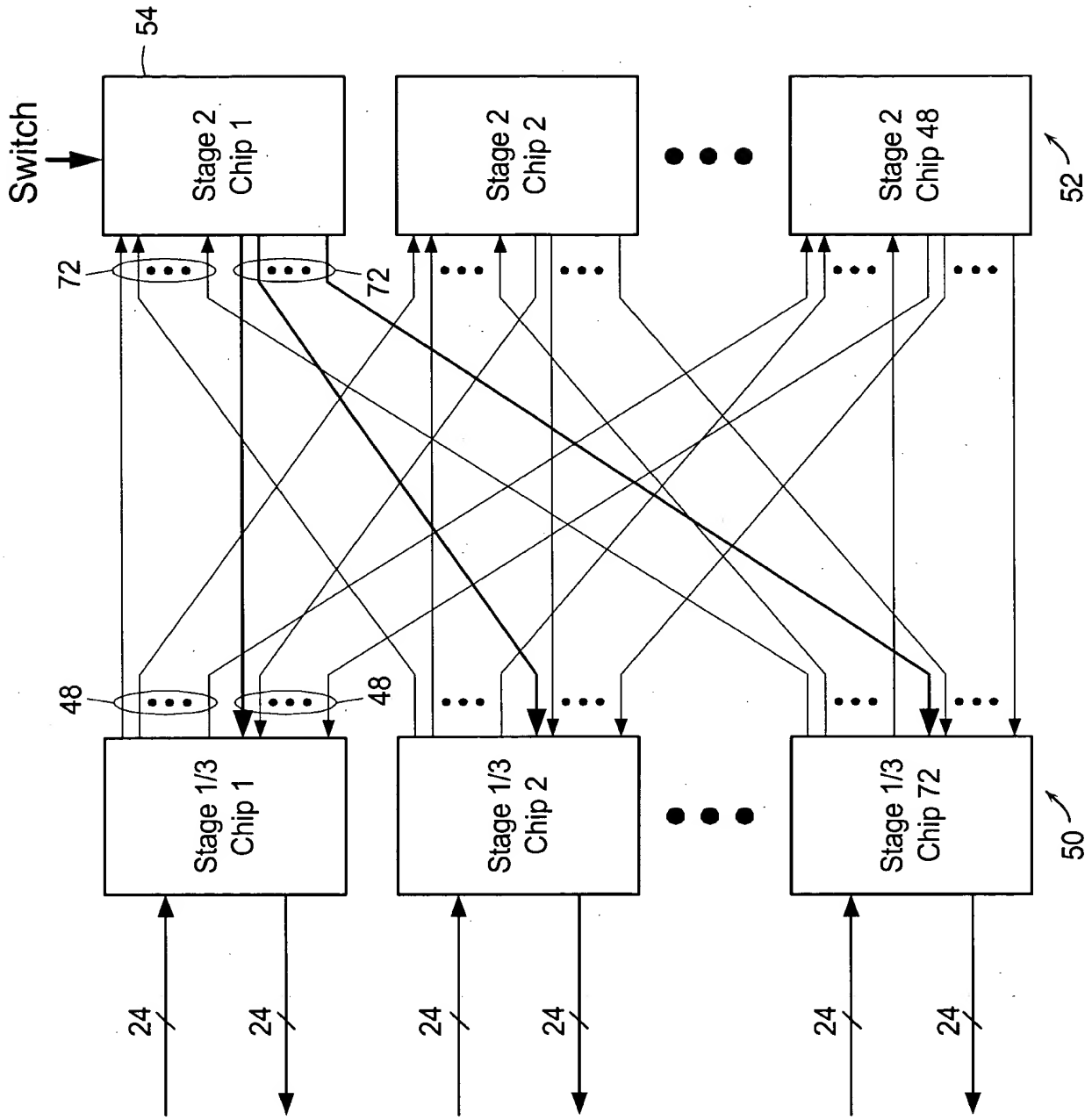
Switch
54
Stage 2 Chip 1
Stage 2 Chip 2
Stage 2 Chip 48
52
72
72
48
48
Stage 1/3 Chip 1
Stage 1/3 Chip 2
Stage 1/3 Chip 72
50
24
24
24
24
24
24

FIG. 8

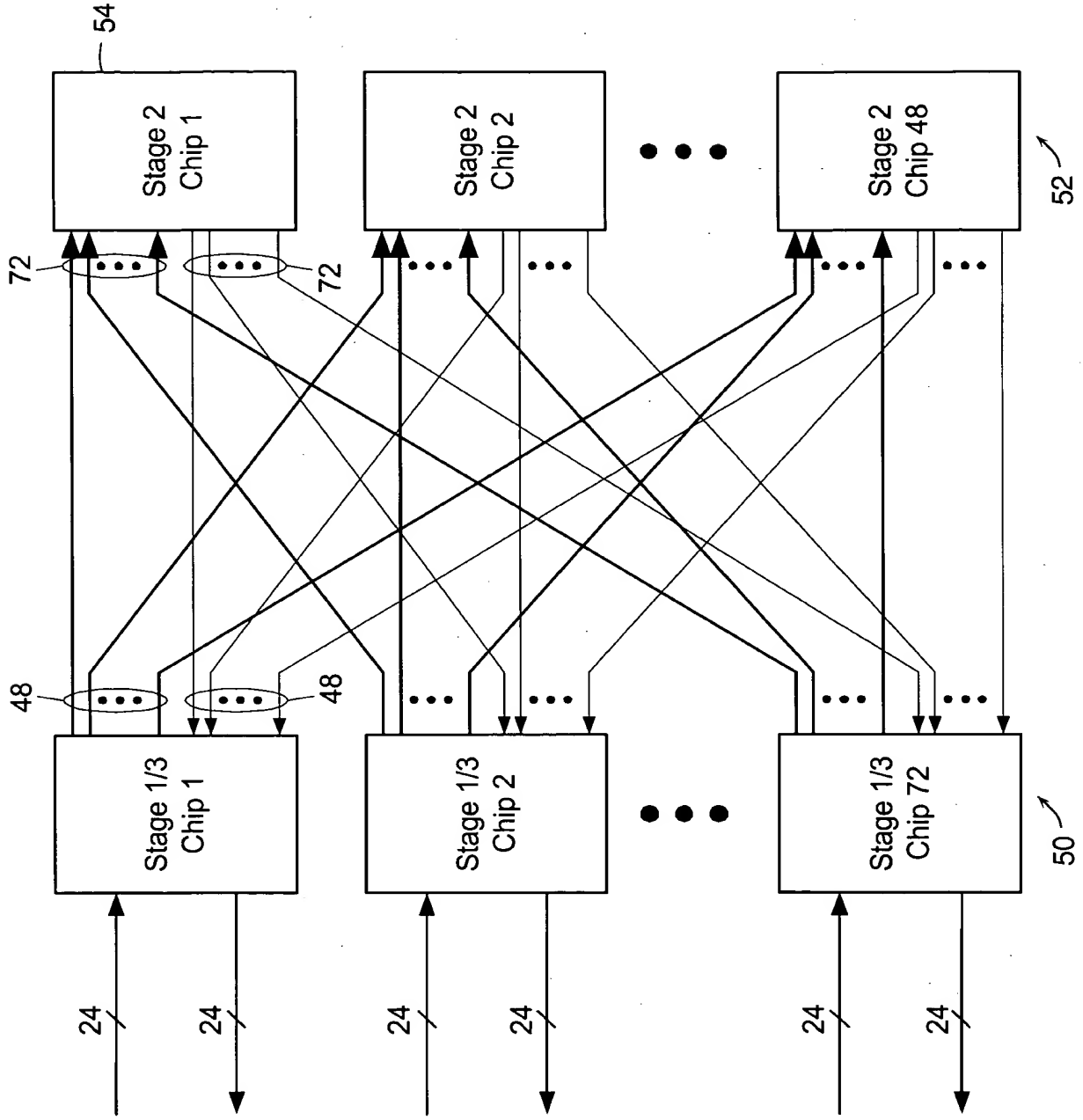
54
Stage 2 Chip 1
Stage 2 Chip 2
Stage 2 Chip 48
52
72
72
48
48
Stage 1/3 Chip 1
Stage 1/3 Chip 2
Stage 1/3 Chip 72
50
24
24
24
24
24
24

FIG. 9

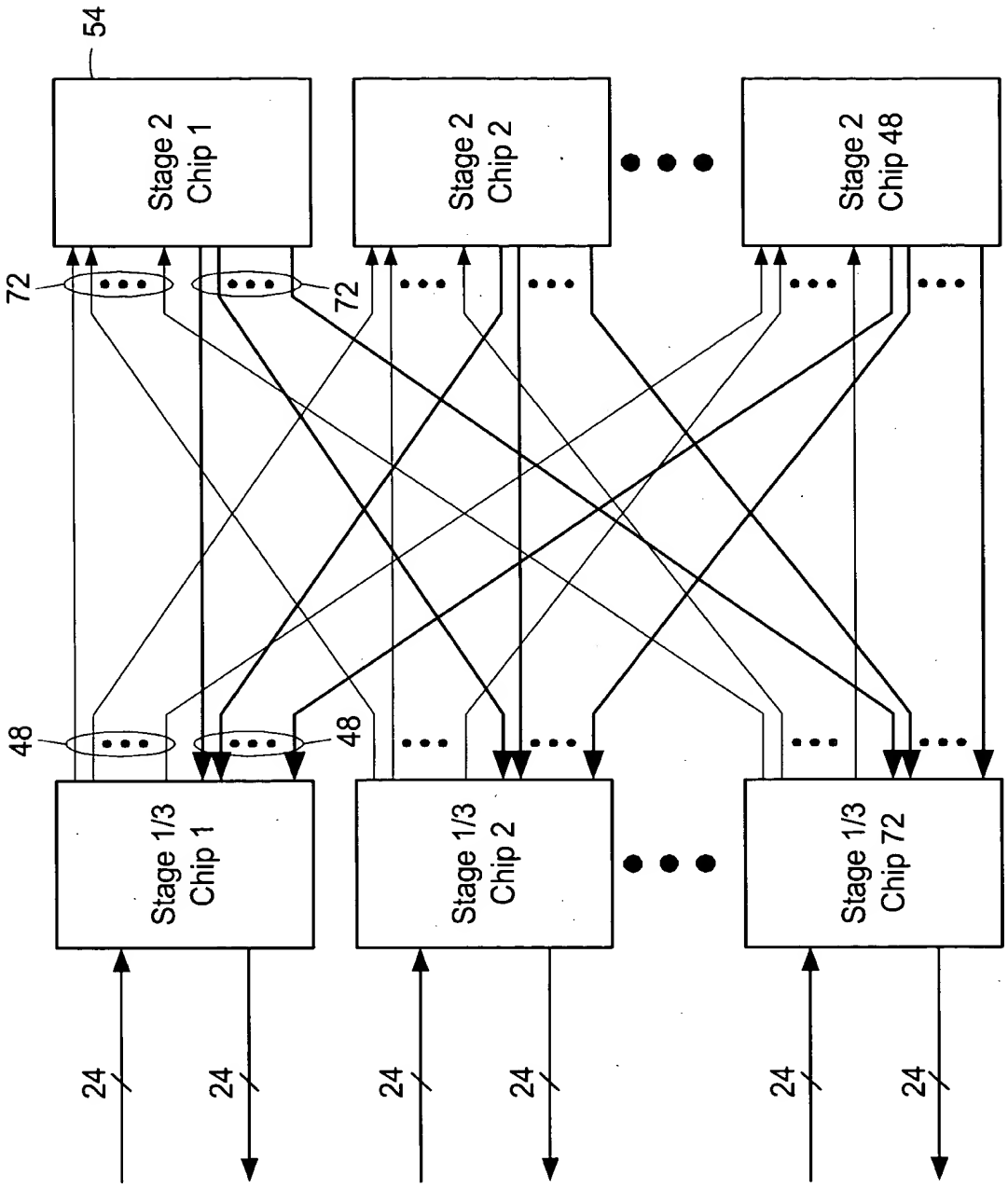
54
Stage 2 Chip 1
Stage 2 Chip 2
Stage 2 Chip 48
72
72
48
48
Stage 1/3 Chip 1
Stage 1/3 Chip 2
Stage 1/3 Chip 72
24
24
24
24
24
24

FIG. 10

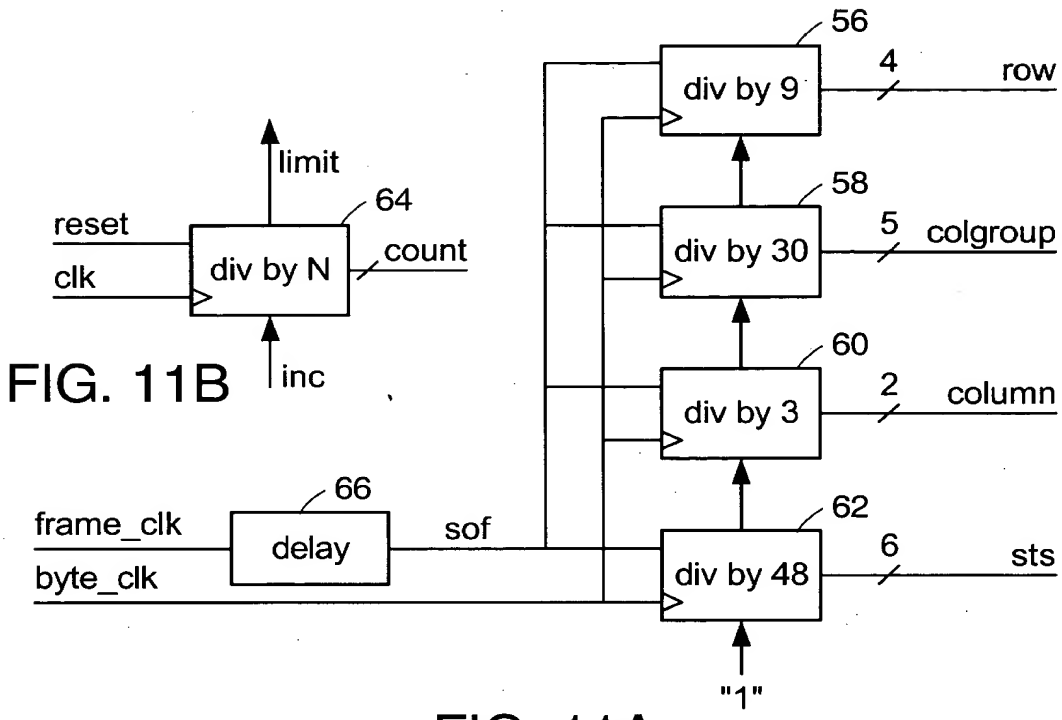

FIG. 11B

FIG. 11A

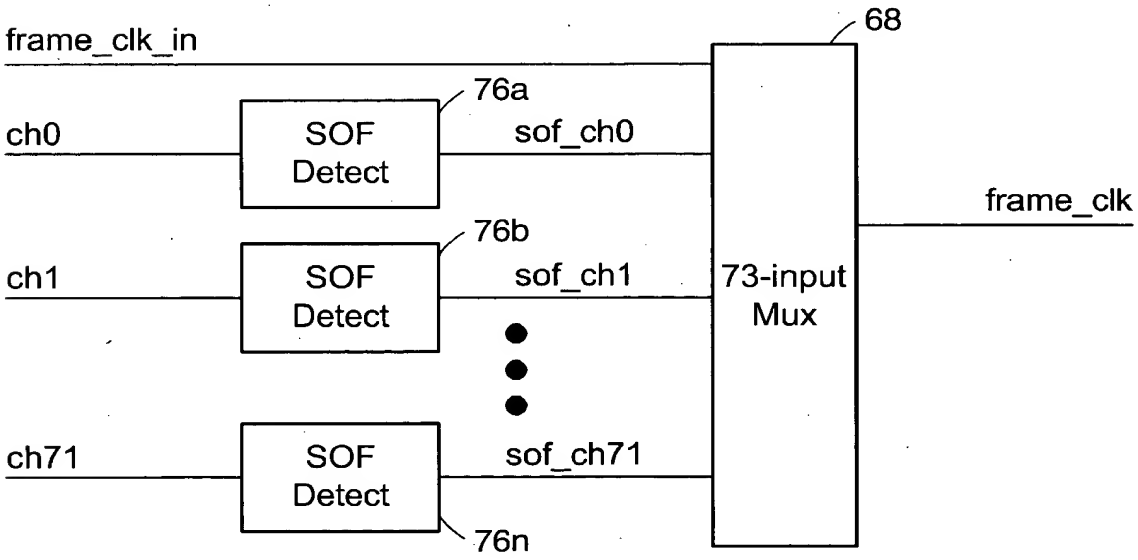

FIG. 12

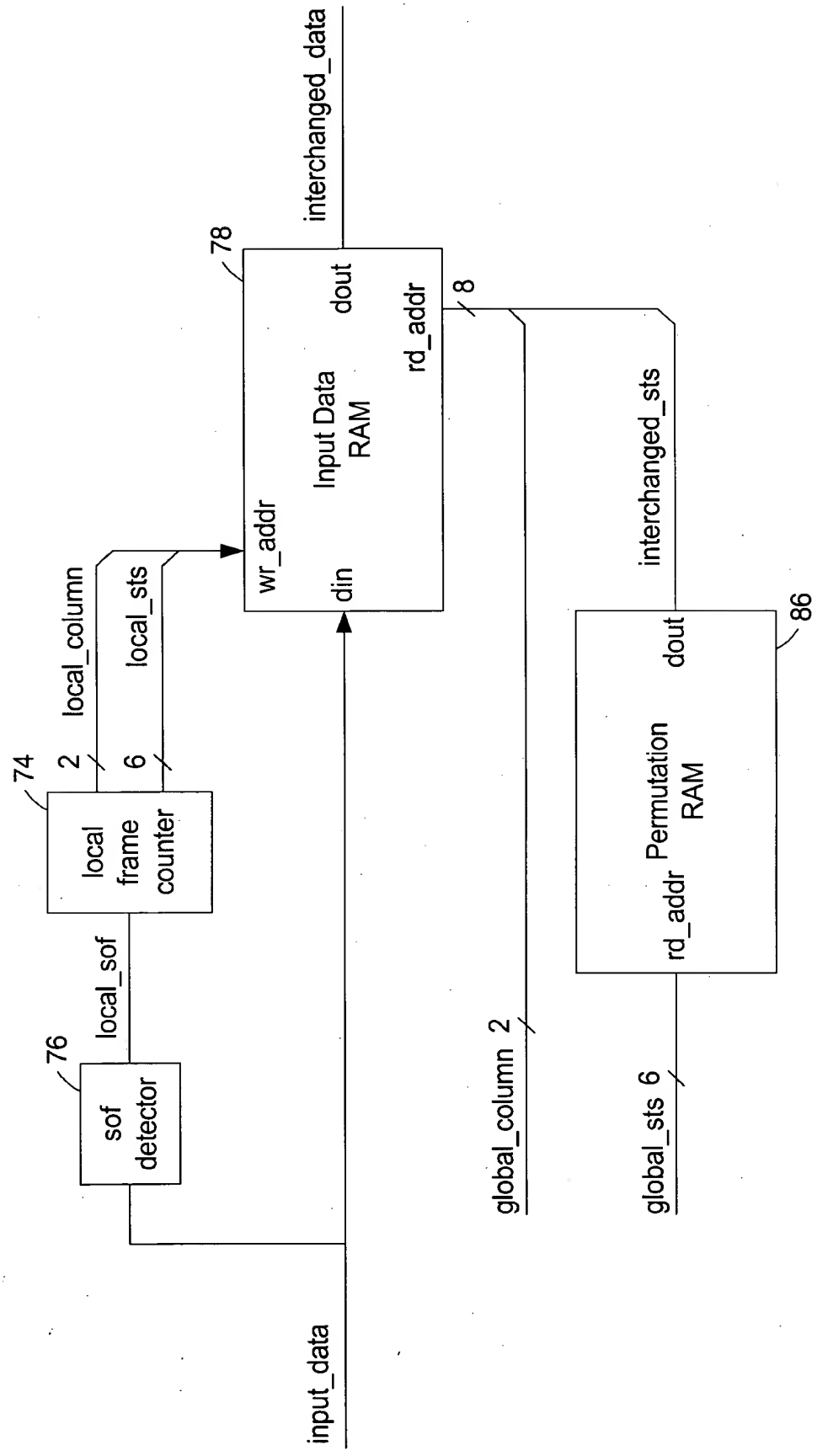
interchanged_data
78
dout
rd_addr
8
Input Data RAM
wr_addr
din
local_column
local_sts
2
6
74
local frame counter
local_sof
76
sof detector
input_data
global_column 2
interchanged_sts
86
dout
Permutation RAM
rd_addr
global_sts 6

FIG. 15

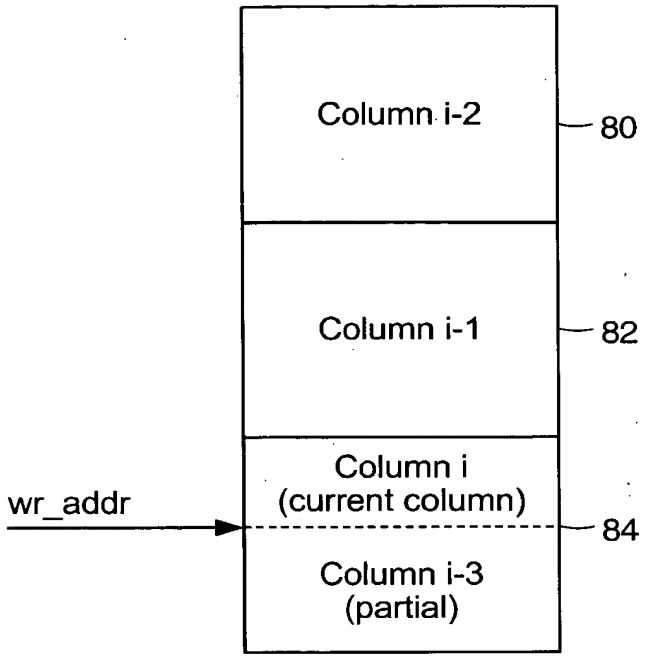
Column i-2
80
Column i-1
82
Column i
(current column)
wr_addr
84
Column i-3
(partial)

FIG. 16

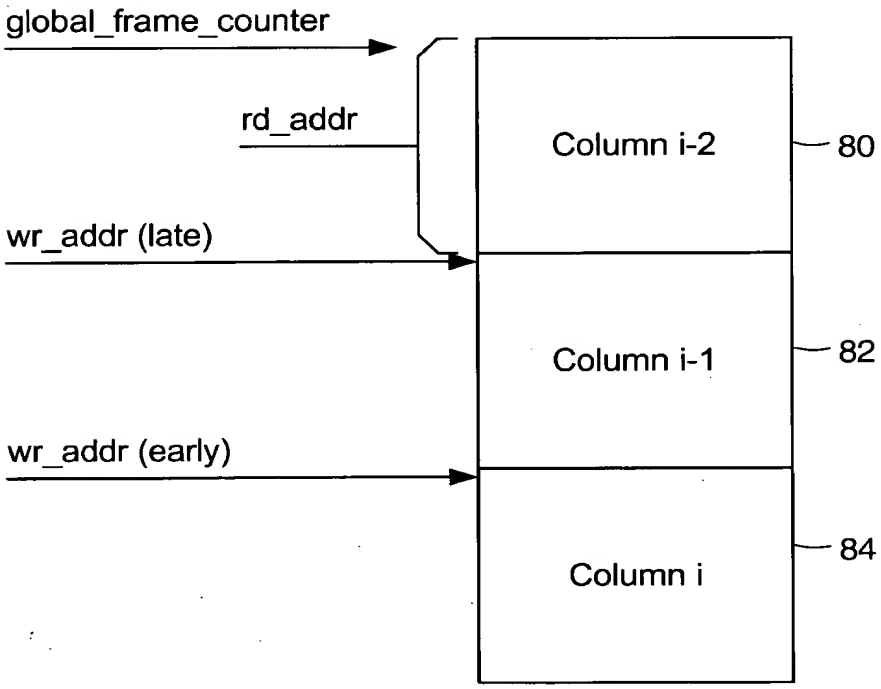
global_frame_counter
rd_addr
Column i-2
80
wr_addr (late)
Column i-1
82
wr_addr (early)
Column i
84

FIG. 17

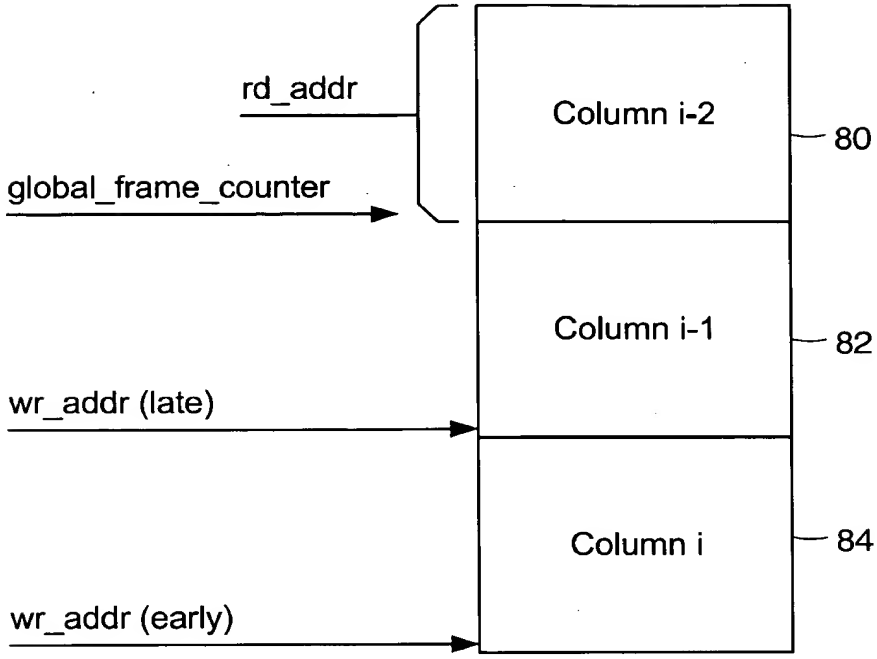
rd_addr
global_frame_counter
Column i-2
80
Column i-1
82
wr_addr (late)
Column i
84
wr_addr (early)

FIG. 18

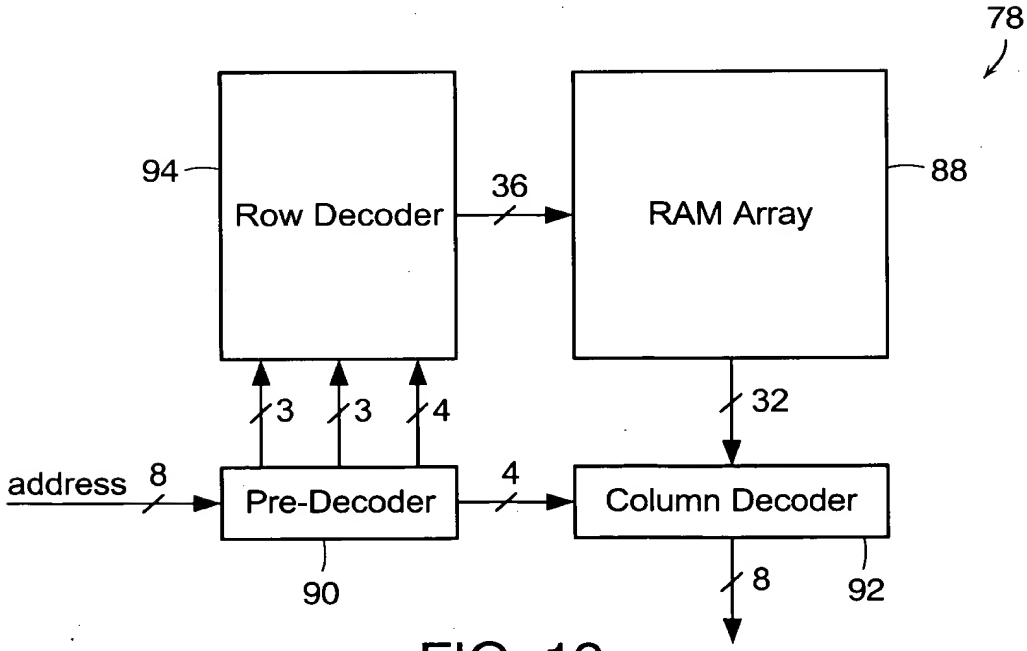
78
94
Row Decoder
36
RAM Array
88
3
3
4
32
address
8
Pre-Decoder
4
Column Decoder
90
8
92

FIG. 19

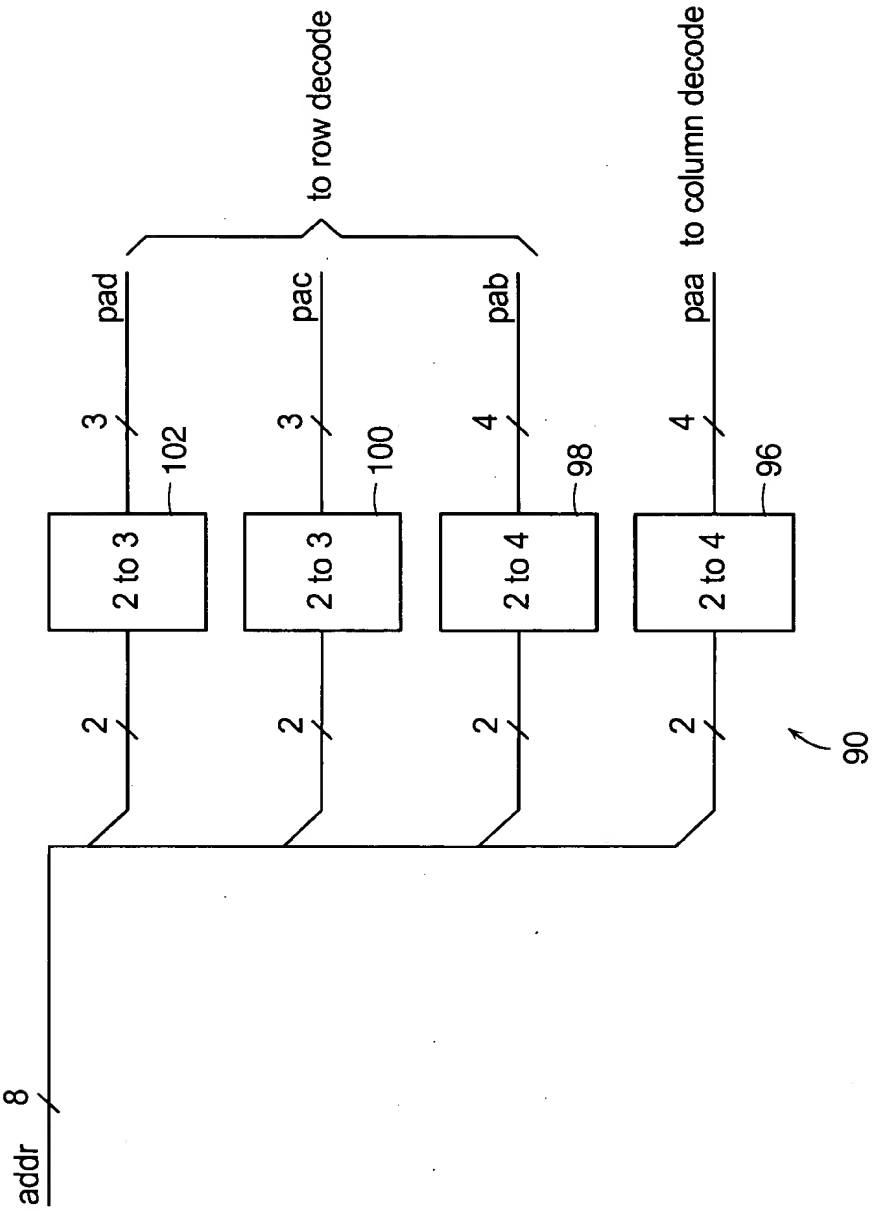
addr
8
2
2 to 3
102
3
pad
2
2 to 3
100
3
pac
2
2 to 4
98
4
pab
2
2 to 4
96
4
paa
to row decode
to column decode
90

FIG. 20

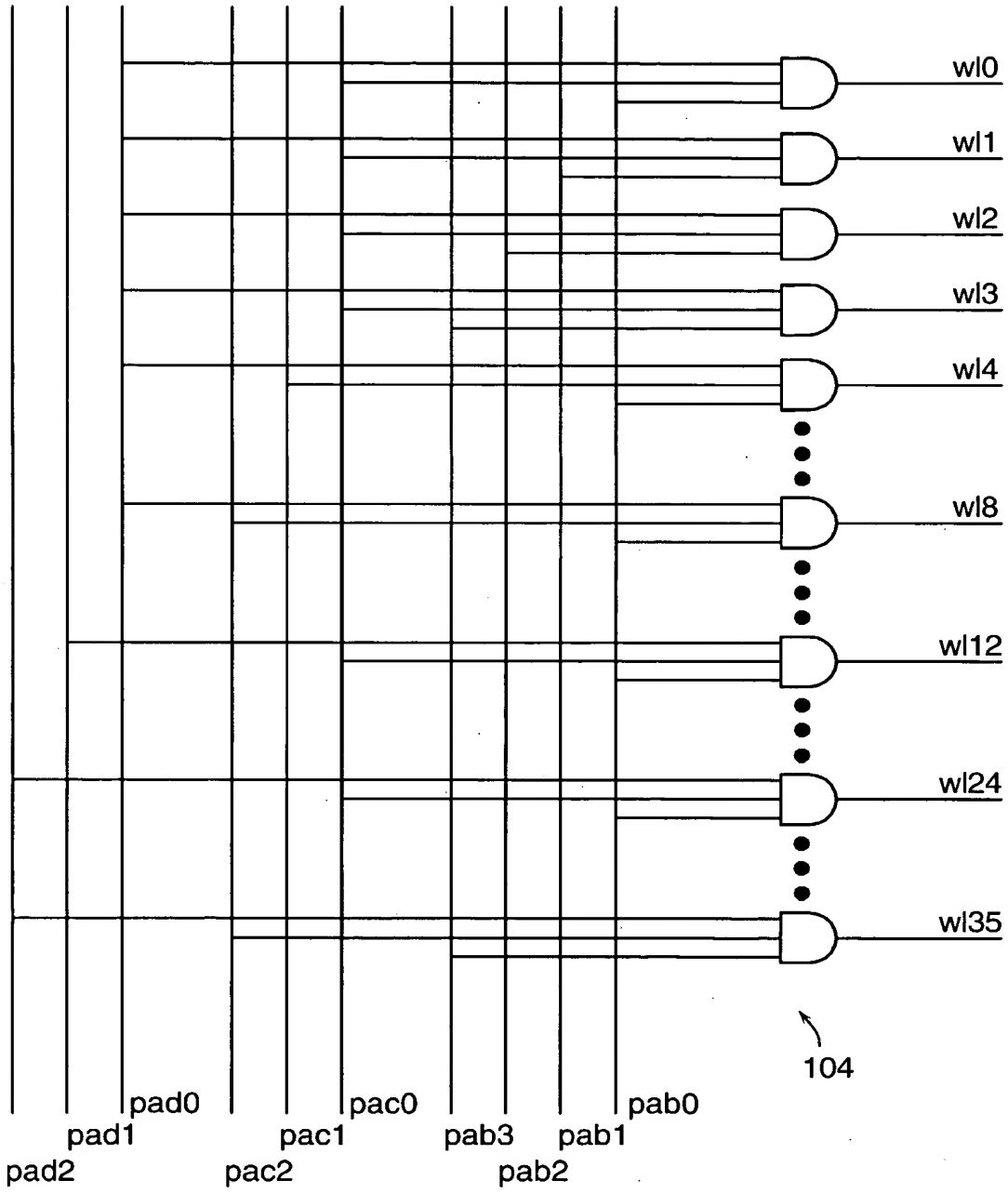
wl0
wl1
wl2
wl3
wl4
wl8
wl12
wl24
wl35
104
pad0
pad1
pad2
pac0
pac1
pac2
pab3
pab2
pab1
pab0

FIG. 21

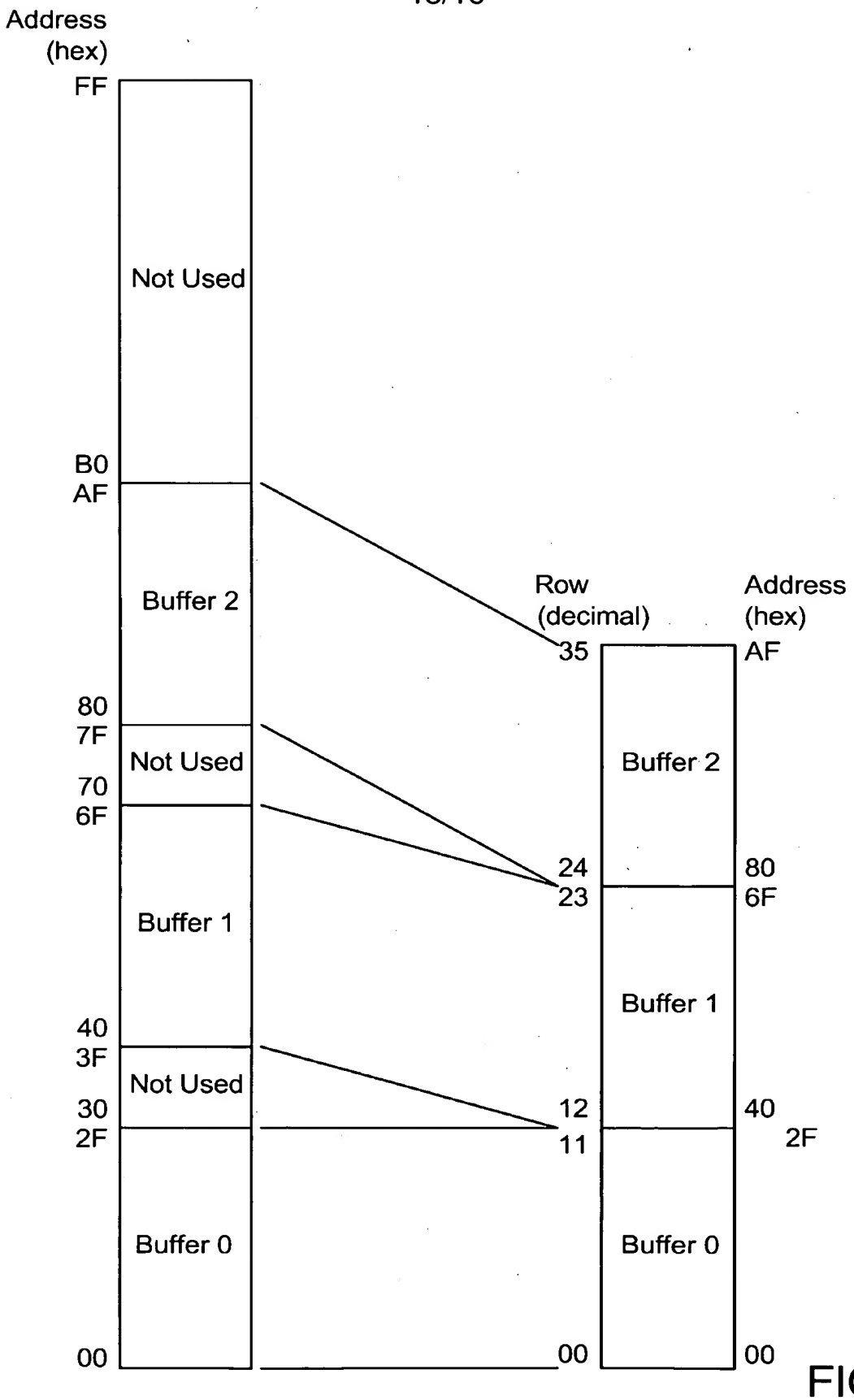
Address
(hex)
FF
Not Used
B0
AF
Buffer 2
80
7F
Not Used
70
6F
Buffer 1
40
3F
Not Used
30
2F
Buffer 0
00
Row
(decimal)
35
24
23
12
11
00
Address
(hex)
AF
Buffer 2
80
6F
Buffer 1
40
2F
Buffer 0
00

FIG. 22

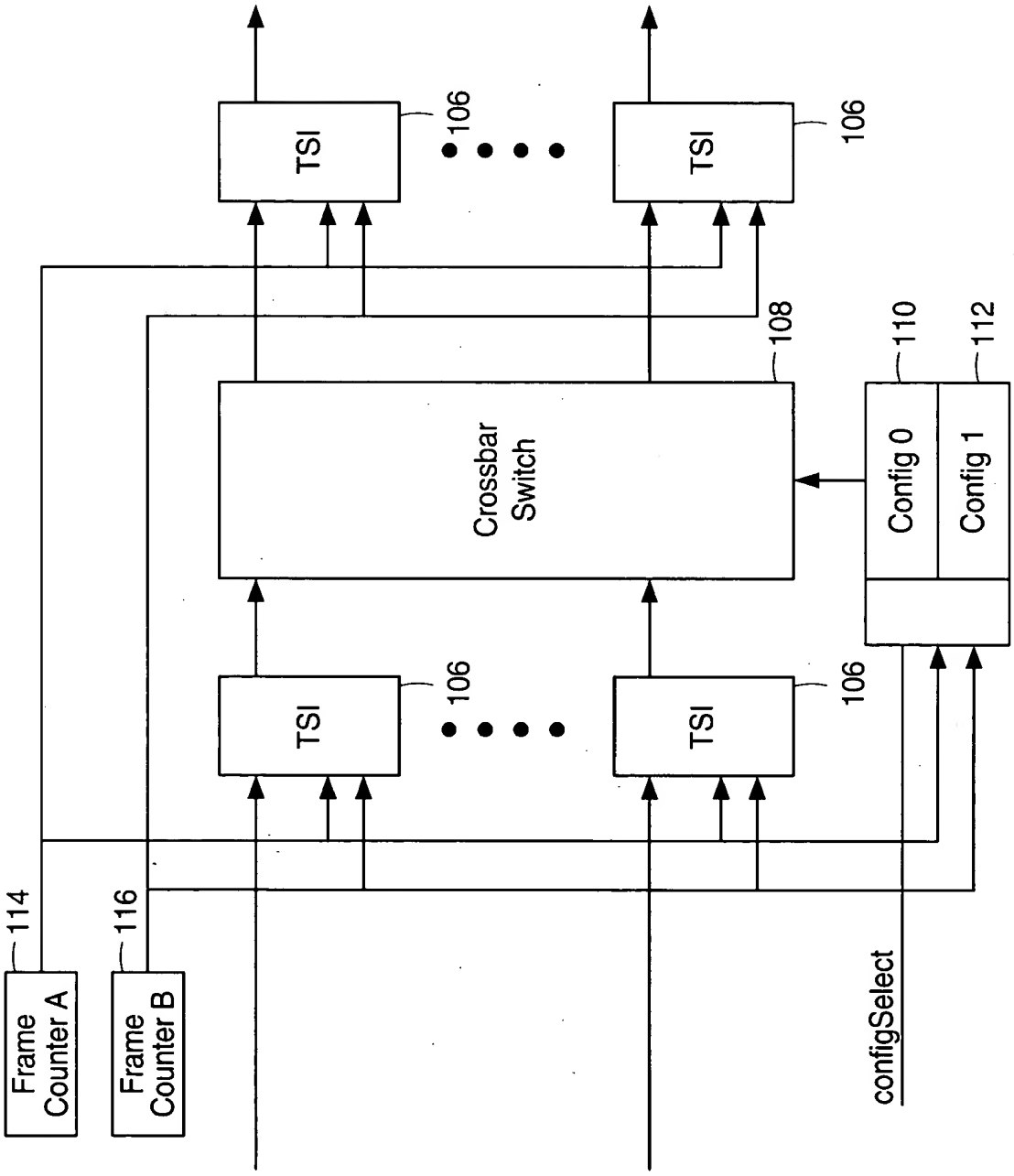
TSI
106
TSI
106
108
110
112
Crossbar Switch
Config 0
Config 1
TSI
106
TSI
106
114
116
Frame Counter A
Frame Counter B
configSelect

FIG. 23